Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

Currently amended claim 2 defines a process of initializing the state of latchable output buffer of a scan cell located at the boundary of a logic circuit within an integrated circuit having a logic circuit.

The process scans data into an input memory circuit of the scan cell while maintaining the scan cell in a first mode that enables connection of the logic circuit to the latchable output buffer.

The process places the scan cell in a second mode that disables connection of the logic circuit to the latchable output buffer.

The process enables transfer of the data scanned into the input memory circuit into the latchable output buffer simultaneous with the placing the cell in a second mode.

The process then disables transfer of the data scanned into the input memory circuit into the latchable output buffer while maintaining the scan cell in the second mode.

In contrast, US 5,281,864 to Hahn discloses a scan cell with a capture section 50 and an update section 52, see Figure 5. The sections respectively include a flip-flop 34 and a flip-flop 36. The text cited in the action states:

In operation, flip-flop 34 is triggered on the positive edge of clock signal TCK and flip-flop 36 is triggered on the negative edge of flip-flop TCK. If there is no requirement to capture data in capture section 50, then data is merely circulated from the output of flip-flop 34 back via multiplexer 54 to the input of flip-flop 34. If however data clock signal CKDR is operative to select the data in signal, then new data will be captured in the flip-flop in response to clocking by the common clock signal. Similarly, for update section 56, data is circulated within the update section until such time as the gated clock signal UDDR operates to select the input of multiplexer 56 which is coupled to the output of capture section 52. (Column 3, line 68 through column 4, line 11)

The Hahn patent fails to teach or disclose any output buffer connected to the output of the multiplexer 32.

The Action recognizes that the Hahn patent does not explicitly disclose initializing the state of the output memory, now the latchable output buffer.

Amended claim 2 requires placing the scan cell in a second mode that disables connection of the logic circuit to the latchable output buffer; enabling transfer of the data scanned into the input memory circuit into the latchable output buffer simultaneous with the placing the cell in a second mode; and thereafter, disabling transfer of the data scanned into the input memory circuit into the latchable output buffer while maintaining the scan cell in the second mode.

US 4,831,623 to Terzian is cited for disclosing transmission gates in place of multiplexers.

Amended claim 2 requires placing the scan cell in a second mode that disables connection of the logic circuit to the latchable output buffer; enabling transfer of the data scanned into the input memory circuit into the latchable output buffer simultaneous with the placing the cell in a second mode; and thereafter, disabling transfer of the data scanned into the input memory circuit into the latchable output buffer while maintaining the scan cell in the second mode.

Claim 2 stands allowable over the cited art.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,

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